What is claimed is:

1. A method for forming a bottle-shaped trench, comprising the steps of:

forming a trench in a substrate;

filling a lower portion of the trench with a conductive layer surrounded by a doped layer;

forming a conformable silicon nitride layer overlying the substrate and an inner surface of an upper portion of the trench to cover the conductive layer and the doped layer;

performing a heat treatment on the substrate to form a doping region therein and around the doped layer;

anisotropically etching the silicon nitride layer to form a collar silicon nitride layer over the sidewall of the upper portion of the trench;

successively removing the conductive layer and the doped layer using the collar silicon nitride layer as a mask to expose the surface of the doping region;

partially oxidizing the exposed doping region to form a doped oxide region thereon;

removing the doped oxide region to form a bottle-shaped trench; and

forming a conformable rugged polysilicon layer in the lower portion of the bottle-shaped trench.

2. The method as claimed in claim 1, further performing a gas phase doping (GPD) after the rugged polysilicon layer is formed.

3. The method as claimed in claim 2, wherein the conductive layer is a polysilicon layer.

4. The method as claimed in claim 1, wherein the doped layer is an arsenic silicate glass (ASG) layer.

5. The method as claimed in claim 4, wherein the doped layer is removed by vapor hydrofluoric (VHF) acid.

6. The method as claimed in claim 5, wherein the silicon nitride layer has a thickness of about 300 to 400Å.

7. The method as claimed in claim 1, wherein the heat treatment is performed at about 900 to 1100°C.

8. The method as claimed in claim 1, wherein the exposed doping region is partially oxidized by rapid thermal oxidation (RTO).

9. A method for forming a bottle-shaped trench capacitor, comprising the steps of:

providing a substrate covered by a masking layer having an opening therein;

etching the substrate under the opening to form a trench therein;

filling a lower portion of the trench with a polysilicon layer surrounded by a doped silicon oxide layer;

forming a conformable silicon nitride layer overlying the masking layer and an upper portion of the inner surface of the trench to cover the

polysilicon layer and the doped silicon oxide layer;

performing a heat treatment on the substrate to form a doping region therein and around the doped silicon oxide layer to serve as a buried bottom plate;

anisotropically etching the silicon nitride layer to form a collar silicon nitride layer over the upper portion of the sidewall of the trench;

successively removing the polysilicon layer and the doped silicon oxide layer using the collar silicon nitride layer as a mask to expose the surface of the doping region;

partially oxidizing the exposed doping region to form a doped oxide region thereon;

removing the doped oxide region to form a bottle-shaped trench;

successively forming a conformable rugged polysilicon layer and a conformable capacitor dielectric layer in the lower portion of the bottle-shaped trench ; and

filling the lower portion of the bottle-shaped trench with a first doped polysilicon layer to serve as a top plate.

10. The method as claimed in claim 9, further comprising the steps of:

removing the collar silicon nitride layer;

forming a collar silicon oxide layer over the upper portion of the sidewall of the bottle-shaped trench; and

successively filling the upper portion of the bottle-shaped trench with a second doped polysilicon layer and a third doped polysilicon layer.

11. The method as claimed in claim 9, wherein the masking layer is composed of a pad oxide layer and an overlying silicon nitride layer.

12. The method as claimed in claim 11, before filling the polysilicon layer, further comprising the steps of:

isotropically etching the pad oxide layer to form a recess with a predetermined depth; and

filling the recess with silicon nitride.

13. The method as claimed in claim 12, wherein the predetermined depth is about 15 to 40Å.

14. The method as claimed in claim 9, wherein the doped silicon oxide layer is an arsenic silicate glass (ASG) layer.

15. The method as claimed in claim 14, wherein the doped silicon oxide layer is removed by vapor hydrofluoric (VHF) acid.

16. The method as claimed in claim 9, wherein the silicon nitride layer has a thickness of about 300 to 400Å.

17. The method as claimed in claim 9, wherein the heat treatment is performed at about 900 to 1100°C.

18. The method as claimed in claim 9, wherein the exposed doping region is partially oxidized by rapid thermal oxidation (RTO).

19. The method as claimed in claim 9, wherein the capacitor dielectric layer comprises a silicon nitride layer.

20. The method as claimed in claim 9, further performing a gas phase doping (GPD) after the rugged polysilicon layer is formed.